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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,667	07/29/2003	Timothy E. Fiscus	0325.00519c	6489

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EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,667	FISCUS ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27,28 and 31* is/are allowed.

6)☒ Claim(s) *1-3,5-8,10-19 and 21-26* is/are rejected.

7)☒ Claim(s) *4,9,20,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The papers filed on 10-03-05 have been received and entered. Claims 1-31 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-3, 5-8, 10-19, 21-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi et al. (U.S. Patent 6,381,188).

Regarding claim 1, Choi teaches a method for reducing power consumption during background operations in a memory array with a plurality of sections (201_1 to 201_4 in figure 2) comprising the steps of: controlling said background operations (refresh operations) in each of said plurality of sections of said memory array response to one or more control signals (PREFs), wherein said background operations can be enabled simultaneously in two or more of said plurality of sections independently of any other section (column 10, lines 26-58); and presenting said one or more control signals

and one or more decoded address signals (DRAs) to one or more periphery array circuits (203s, 219) of said plurality of sections.

Regarding claim 2, Choi teaches the background operations comprise a refresh operation (column 4, lines 12-16).

Regarding claim 3, Choi teaches the plurality of sections comprise quadrants (There are shown four banks 201s in figure 2; column 4, lines 22)

Regarding claim 5, Choi teaches a step of controlling in response to said one or more control signals, an operation of said one or more periphery array circuits, wherein said periphery array circuits each comprise one or more circuits from the group consisting sense amplifiers, column multiplexer circuits, equalization circuits, and wordline driver circuits (each periphery circuit includes all these circuits for operating a memory bank).

Regarding claim 6, Choi teaches generating one of said one or more control signals (PREFs in figure 2) for each of said plurality of sections of said memory array.

Regarding claim 7, Choi teaches the one or more control signals (PREFs) are generated in response to an address signal (A1~An in figure 2).

Regarding claim 8, Choi teaches a step of generating said one or more control signals (PREFs) in response to a refresh enable signal (RCON1/RCON2).

Regarding claim 24, Choi teaches said one or more decoded address signals comprise one or more decoded row address signals and one or more decoded column address signals (DRAs).

Regarding claim 25, Choi teaches said background operations (refresh) are enabled in response to a first state of said one or more control signals (when signal PREFs are activated)

Regarding claim 26, Choi teaches said background operations are disabled response to a first state of said one or more control signals (when signal PREFs are in logic low level).

Regarding claims 10 and 11, Choi teaches an apparatus comprising: a memory array (figure 2) comprising a plurality of sections (201_1 to 201_4), wherein each of said sections comprises (i) a plurality of memory cells (in memory banks) and periphery

array circuitry (including 203, 205) configured to control access to said plurality of memory cells; and a control circuit (213) configured to present one or more control signals (PREFs) and one or more decoded address signals (DRAs) to said periphery array circuitry of said plurality of sections, wherein a background operation (refresh operation) in each of said plurality of sections controlled in response to said one or more control signals and said background operation can be enabled simultaneously in two or more of said plurality of sections independently of any other section (column 10, lines 26-58).

Regarding claim 12-19, 21-23, they recite similar limitations as the claims 1-8 and 24-26 and therefore are rejected for the same reasons.

Allowable Subject Matter

4. Claims 27, 28 and 31 are allowed.

5. Claims 4, 9, 20, 29 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Choi and the prior art of record fail to teach the further limitation of the background operations comprising parity checking.

Response to Arguments

7. Applicant's arguments filed 10-03-05 have been fully considered but they are not persuasive. In the Remarks, pages 11 and 12, the Applicants argued that "Choi does not disclose or suggest that the background operations can be enabled simultaneously in two or more of the plurality of sections independently of any other section, as presently claimed." The Applicants further argued that "Choi discloses that a refresh

operation must occur in memory banks one and two when a refresh operation occurs in memory banks three and four". The Examiner would like to direct the Applicants to column 10, lines 47-50 of Choi which states: "Thus, the first through third memory banks 201_1, 201_2 and 201_3 perform a refresh operation and the fourth memory bank 201_4 does not perform a refresh operation." In other words, the first through third memory banks are enabled simultaneously and independently of the fourth bank. To the second point raised by the Applicants, the Examiner does not see how the argument is relevant to the claimed invention. Since this limitation is not included in claims 1, 10 and 11, it is irrelevant if Choi teaches the limitation or not. In conclusion, claims 1-3, 5-8, 10-19, 21-26 are unpatentable over Choi.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11-03-05

Son L. Mai
Primary Examiner
Art Unit 2827